PRG

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/395,294	09/13/1999	SOPHIE WILSON	1073/OG117	5796

7590 04/03/2003

DARBY & DARBY PC
805 THIRD AVENUE
NEW YORK, NY 10022

EXAMINER
MEONSKE, TONIA L

ART UNIT	PAPER NUMBER
2183	16

DATE MAILED: 04/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/395,294	WILSON, SOPHIE	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 14 depends from cancelled claim 13. For purposes of examination it is assumed that Applicant intended claim 14 to depend from claim 12 instead of claim 13.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 7, and 8 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Shiell et al., US Patent 6,317,820, cited as prior art reference in paper number 6, mailed on January 15, 2002.

5. Referring to claim 1, Shiell et al. have taught a computer system comprising:

a. a decode unit (Figure 1, element 115) for decoding instructions fetched from a memory (Figure 1, element 105) holding a sequence of instructions (Figure 1, abstract,

column 3, lines 5-15, column 4, lines 1-9), all instructions in the sequence having the same predetermined bit length (column 3, lines 5-15); and

b. first and second processing channels (column 3, lines 54-58, A side and B side), each channel comprising a plurality of functional units, at least one of said functional units in each channel being a data processing unit (column 3, lines 56-61, S, L, and M units) and at least one other of said functional units in each channel being a memory access unit (column 3, lines 56-61, D unit);

c. wherein the decode unit is operable to detect for each instruction of said predetermined bit length whether the instruction defines a single operation or two independent operations and to control the first and second channels in dependence on said detection (column 2, lines 23-56).

6. Referring to claim 2, Shiell et al. have taught a computer system according to claim 1, as described above, and wherein, when the decode unit detects that the instruction defines two independent operations (column 2, lines 23-56, Second mode), it is operable to control the first channel to implement one of those operations (column 2, lines 23-56, A side operation) and the second channel to implement the other of those operations (column 2, lines 23-56, B side operation), whereby the first and second channels execute their respective independent operations simultaneously (column 2, lines 23-56).

7. Referring to claim 3, Shiell et al. have taught a computer system according to claim 1, as described above, and wherein when the decode unit detects that the instruction defines a single operation, it controls the first and second channels each to cooperate to simultaneously execute said single operation (column 2, lines 23-56, First mode).

8. Referring to claim 4, Shiell et a. have taught a computer system according to claim 1, wherein the first and second channels share at least one common register file and can simultaneously access said register file (column 4, lines 24-34, Figure 1, elements 140a and 140b).

9. Referring to claim 7, Shiell et al. have taught a computer system according to claim 1, as described above, and wherein the decode unit is operable to identify certain combinations of said independent operations in an instruction based on said set of identification bits,

a. wherein a first combination denotes two data processing operations (Column 2, lines 23-56, column 3, line 50-column 4, line 9, Second Mode, This combination is identified when an instruction from side A and an instruction from side B are dispatched to either the S, L, or M functional units.),

b. a second combination denotes two memory access operations (Column 2, lines 23-56, column 3, line 50-column 4, line 9, Second Mode, This combination is identified when an instruction from side A and an instruction from side B are dispatched to the D functional units.),

c. a third combination denotes a data processing operation and a memory access operation (Column 2, lines 23-56, column 3, line 50-column 4, line 9, Second Mode, This combination is identified when an instruction from side A is dispatched to either the S, L, or M functional unit and when an instruction from side B is dispatched to the D functional unit.), and

d. a fourth combination denotes a long instruction (Column 2, lines 23-56, column 3, line 50-column 4, line 9, An instruction dispatched in the First Mode.).

10. Claim 8 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

11. Claim 16 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yoshida, US Patent 5,761,470.

12. Referring to claim 16, Yoshida has taught a computer program product comprising program code means which include a sequence of the instructions all having the same predetermined bit length (column 19, lines 61-65), said instructions including long instructions wherein said predetermined bit length defines a single operation (Figure 25, element 502) and dual operation instructions wherein said predetermined bit length defines two independent operations (Figure 25, element 501), said instructions including a set of identification bits at designated bit locations within the instruction (Figure 25, elements 505 and 506), wherein the computer program product is adapted to run on a computer such that said identification bits are adapted to cooperate with a decode unit of the computer to designate whether:

a) the instruction is a long instruction (Figure 26, FM = 1-) or a dual operation instruction (Figure 26, FM = 00 and FM = 01); and

b) in the case of a dual operation instruction, the nature of each operation in the instruction selected from a data processing category and a memory access category (column 7, lines 1-36, column 19, line 65-column 20, line 4).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 5, 6, 9, 10, 11, 12, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell et al., US Patent 6,317,820, cited as prior art reference in paper number 6, mailed on January 15, 2002, in view of Yoshida, US Patent 5,761,470.

15. Referring to claim 5, Shiell et al, have taught a computer system according to claim 1, as described above. Shiell et al. have not specifically taught wherein the decode unit is operable to make said detection based on the values of a designated set of identification bits at predetermined bit locations in the instruction. However, Yoshida has taught wherein the decode unit is operable to make said detection based on the values of a designated set of identification bits at predetermined bit locations in the instruction (Figure 25, elements 505 and 506). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instructions of Shiell et al. make said detection based on the values of a designated set of identification bits at predetermined bit locations in the instruction, as taught by Yoshida, in order to easily determine whether the bit length defines a single operation or two independent operations. Having the designated bits at predetermined bit locations in the instruction itself would eliminate the need to have a separate instruction (Shiell et al., column 2, lines 53-55) preceding the instruction in order to set up the channels for execution.

16. Referring to claim 6, Shiell et al. and Yoshida have taught a computer system according to claim 5, as described above and wherein, when the instruction has a length of n bits (Yoshida, Figure 25, element 501s and 502), the predetermined bit locations include the n/2th bit (Yoshida, Figure 25, element 506, counting from right to left of the bits in instruction 501) and the nth bit (Yoshida, Figure 25, element 505, counting from right to left of the bits in instruction 501).

17. Claim 9 does not recite limitations above the claimed invention set forth in claim 5 and is therefore rejected for the same reasons set forth in the rejection of claim 5 above.

18. Claim 10 does not recite limitations above the claimed invention set forth in claim 5 and is therefore rejected for the same reasons set forth in the rejection of claim 5 above.

19. Claim 11 does not recite limitations above the claimed invention set forth in claim 6 and is therefore rejected for the same reasons set forth in the rejection of claim 6 above.

20. Referring to claim 12, Shiell et al. have taught a computer program product comprising

a. program code means which include a sequence of instructions all having the same predetermined bit length (column 3, lines 5-15), said instructions including long instructions wherein said predetermined bit length defines a single operation (column 2, lines 23-56, First mode) and dual operation instructions (column 2, lines 23-56, Second mode), wherein said predetermined bit length defines two independent operations (column 2, lines 23-56, Second mode),

b. wherein the computer program product is adapted to run on a computer such that a long instruction defining a single operation controls the resources of the computer in a first way (column 2, lines 23-56, First mode) and a dual operation instruction defining two independent operations controls the resources of the computer in a second way (column 2, lines 23-56, Second mode).

21. Shiell et al. have not taught each instruction of said predetermined bit length includes a set of identification bits at designated bit locations within the instruction, said identification bits being adapted to cooperate with a decode unit of a computer system to designate whether the instruction is a long instruction or a dual operation instruction. Yoshida has taught each

instruction of said predetermined bit length includes a set of identification bits at designated bit locations within the instruction (Figure 25, elements 505 and 506), said identification bits being adapted to cooperate with a decode unit of a computer system to designate whether the instruction is a long instruction or a dual operation instruction (Figure 25, Figure 26, FM). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have each instruction of Shiell et al. contain a set of designated bits at designated bit locations within the instruction, as taught by Yoshida, in order to easily determine whether the instruction is a long instruction or a dual instruction operation. Having the designated bits at predetermined bit locations within the instruction itself would eliminate the need to have a separate instruction (Shiell et al., column 2, lines 53-55) preceding the instruction in order to set up the mode of execution of the instruction.

22. Claim 14 does not recite limitations above the claimed invention set forth in claim 6 and is therefore rejected for the same reasons set forth in the rejection of claim 5 above.

23. Referring to claim 15, Shiell et al. have taught a method of operating a computer system which comprises first and second processing channels (column 3, lines 54-58, A side and B side) each having a plurality of functional units (column 3, lines 56-61, S, L, M and D units) including at least one data processing unit (column 3, lines 56-61, S, L, and M units) and one memory access unit (column 3, lines 56-61, D unit), the method comprising:

a. fetching a sequence of instructions from a program memory (column 3, lines 5-15), all said instructions having the same predetermined bit length (column 3, lines 5-15);

b. decoding each instruction (Figure 1, element 115), and said decoding determining:

a) whether the instruction of said predetermined bit length defines a single operation or two independent operations (column 2, lines 23-56); and

b) where the instruction of said predetermined bit length defines two independent operations, the nature of each of those operations selected at least from a data processing category of operation and a memory access category of operation (column 7, lines 1-36, column 19, line 65-column 20, line 4).

24. Shiell et al. have not taught the instructions containing a set of designated bits at predetermined bit locations within said bit length and said decoding step including reading the values of said designated bits to determine steps a) and b) above. However Yoshida has taught instructions containing a set of designated bits at predetermined bit locations within said bit length (Figure 25, elements 505 and 506) and said decoding step including reading the values of said designated bits to determine steps a) (Figure 25, Figure 26, FM) and b) (column 7, lines 1-36, column 19, line 65-column 20, line 4) above. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instructions of Shiell et al. contain a set of designated bits at predetermined bit locations within said bit length, as taught by Yoshida, in order to easily determine whether the bit length defines a single operation or two independent operations. Having the designated bits at predetermined bit locations in the instruction itself would eliminate the need to have a separate instruction (Shiell et al., column 2, lines 53-55) preceding the instruction in order to set up the channels for execution.

Response to Arguments

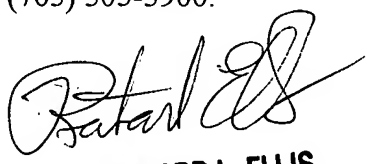
25. Applicant's arguments with respect to claims 1-12 and 14-16 are but are moot in view of the new ground(s) of rejection.

Conclusion

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 9-6:30, with every other Friday off.

27. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

28. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.



RICHARD L. ELLIS
PRIMARY EXAMINER

tlm
April 1, 2003